SOLID STATE SWITCH FOR HIGH RELIABILITY SPACECRAFT USE

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ABSTRACT

The drive to improve interplanetary spacecraft power system reliability and fault tolerance spurred JPL to develop a Solid State. Power Switch (SS['S). JPL began the. development of the SSPS in the late nineteen eighties to replace the traditional mechanical relay/fuse combination with high reliability solid state designs that provide distribute.cl fault protection anrt load switching.

The JPL design was driven by the high reliability, fault tolerant requirements of the Cassini mission to Saturn (late 1997 launch). The Cassini space.craft will be the first JPL spacecraft to utilize a solid state device for power distribution. One. hundred and nine.ty-two (192) SSPS hybrid units will be used to control numerous spacecraft loads. The system approach and design philosophy of the SSPS were previously reported at the (1994), 29th IECEC conference (Dalton, etal.). This paper dc..scribcs the design and implementation of the flight qualified hybridized SS1'S.

INTRODUCTION

The. SSPS is required to provide. reliable operation throughout a long thirteen (13) year mission. nigh reliability was maintained by hybridizing the SSPS in compliance with the K level requirements of MIL-STD 38534.

The Cassini Spacecraft utilize.s a 30V floating (with respect to chassis) power bus, consisting of 30V power and 30V return lines. Cassini will be the first JJ'L spacecraft to utilize the "hard power bus" concept. The hard power bus is defined as a system where a fault on a give.n load is transparent to the othe r user> of the. power bus. Thus, load faults on the hard power bus must be "cleared" (removed from the power bus) without triggering an r-nidcr-voltage (out of regulation) condition on the other users. This fault protection and failure immunity properties of the SSPS arc achieved by a completely redundant design. The SSPS also provides the option (not possible with fuses) of re-energizing a load in the event that a self clearing fault or temporary overload condition has caused the load to "clear". 1 Iybrid design and fabrication were done by CTS Microelectronics, West Lafayette Indiana.

The SSPS is packaged in a hermetically scaled 72 pin, Kovar package measuring 4.06 X 5.33 X 0.63 cm. The total weight of the SSPS hybrid is about 31 gr. It is implemented by thick film technology and utilizes two (for redundancy) semi-custom digital gate-arrays for the command interface.

The SSPS is designed for a 30V spacecraft bus and rated for 3A loads (also has paralleling capability), It can be externally programmed for c ight different load (trip) currents thus catering to a wide range. of loads. In the event of a load short, fault current is limited to 6A followed by turn OFF (TRIP). The SS1'S provides soft turn-on, restart capability and load current status for downlink telemetry. The SSPS can be commanded through either (or both) of two independent serial ports.

SSPS DESIGN

A c ompletely redundant design and implementation assures that ***no single point failure will result in a load staying permanently connected to the bus.*** This design approach resulted in independent bus side and return side circuitry The load is switched by two power FETs. (One on the bus

side and one on the return side).

The Command processor electronics is digital and occupies about half of the switch's discrete elements. in the hybi id, this digital circuitry is implemented by a gate-array (there arc two like die per hybrid unit for redundancy). The switch block diagram is depicted in ***Figure 1.***

Functional **Description:**

Input Logic

The SS1'S will accept commands on either the Bus or the Rtn control input or on both inputs simultaneously. In the event of simultaneous commands, OFF commands arc higher precedence than ON commands. This feature greatly simplifies the. design of the Command System as it permits the usc of two completely independent command data systems with no synchronization required between the two systems.

The SSPS commrrnd format is 16 bit serial. Each SSPS within the Cassini power distribution system is assigned a unique 8 bit address. SSPS commands contain an embedded 8 bit address. All *the* SSPSs monitor the 4 wire command bus. When a command is sent the SSPS address decoder compares the embedded address to the assigned address and if they match the command is processed. Parity and Start Bit arc checked. If Parity, Start f?it and Address arc true the command is accepted. The SSPS simplifies the "system" because a single 4 wire serial command bus is all that is needed to command all the SS1'Ss (Cassini uses two independent command busses for redundancy).

Command Logic

The Bus and Rtn Input Logic each contain a command processor and address decoder to implement the above features Once. accepted, SSPS commands arc latched. The latching function takes place via a state machine contained within the command logic block.

The SSPS can reside in one of 3 state.s; ON, OFF and TRIP. The TRIP state is similar to the OFF state except that the SSPS has been turned OFF by internal control circuitry in response to an overload, rather than by external command.

Switch Subsystem

The. Current Clamp, Over-current Trip and Soft-Start features arc implemented in the (analog) Switch Subsystem. The Switch Subsystem contains closed loop servo control circuitry to implement the Current Clamp feature, comparators, references and D/A convertors to implement the Over-current Programmable Trip function, power MOSFETs and MOSFET bias circuits to realize the ON (soft start) and OFF characteristics.

The SS1'S fault protection works as follows. If load current exceeds a preset (one of eight) value, an internal timer is started, The timer expire-s after 1ms and if the. load current still exceeds the. prc.set value., the SS1'S latches in the. TRIP state. During the 1mS interval load current is actively limited to 6 amps by the SS1'S "Current Clamp" circuit. If the load current drops down below the preset value before the timer expire.s, the timer is reset. The Trip Circuit also contain.. an integrator to handle the. case. of an oscillating faulted load. The integrator time constant is 'Sins.

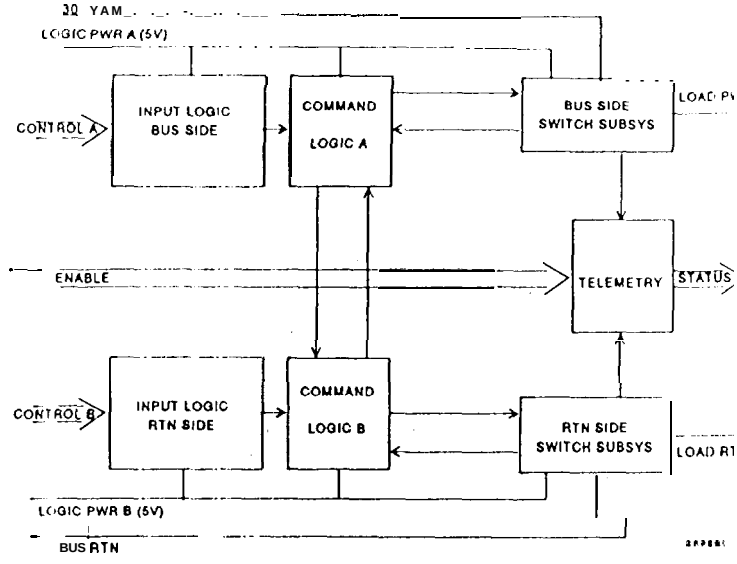

Figure 1. SSPS ***Functional Block*** *Diagram*

The Soft-start feature. is achieved via the usc of a "Miller integrator". The. drain voltage of the MOSFET is fed-back to a high impedance gate. drive circuit through an external capacitor (0.5uF on Cassini). The "Miller" feedback provides a nearly linear rise in drain voltage over time, given a resistive load. Load voltage rise time is about 120mS, *10-90%.*

Telemetry

The SS['S provides switch and load state information for downlink telemeti y in the form of 3 digital and two analog signals. All signals arc buffered to prevent noise from propagating into the. SSPS from external circuitry. Additionally the digital signals arc tri-state and the analog signals arc switched. These feature-s greatly simplify the design of the spacecraft telemetry collection multiplexer.

Design of the SSPS

The SSPS design process was top down. Electronic engineers worked close.ly with the spacecraft power system engineers to draft the switch functional requirements and performance targets.

Electronic design was performed using the "worst case. design" method. "Worst case" part parameters were used to calculate circuit performance during the design phase rather than afterwards. Part parameter variations were taken from a "Worst Case. Parts Paramete r Database" developed try J PL.

Electronic parts were. chose.n from an Approved Parts List (A PI.) developed by J PI. for the Cassini project. Part parameter variations for parts on the APL were automatically included in the Parts parameter Database. Using parts excl usively from the APL was a challenge for the designers but it was beneficial in the. long run, Part problems were minimized and the JPL internal review process was greatly simplified, thus saving money for the project.

The electronic design was simulated and breadboarded for proof of concept and to "flesh out" any potential problems. Next, formal Worst Case Analysis verified the electrical performance. and a discrete. version of the SS1'S was created using conventional PCB technology. The PCB version of the SSPS was tested for electrical performance prior to hybridization. Additionally, testing the PCB facilitated the development of a test plan for the hybrids.

The SS1'S was dc.signed and fabricated to meet the following requirements:

FUNCTIONA LREQUIREMENTS

1. Soft start: 100 ms typical 10-90% voltage rise into a 30 ohm load
2. Eight selectable current trip Levels, 3/8 A to 3 A.
3. 1 ms trip time.
4. 200 us turn OFF time.
5. Load current limited to 6 A by SSPS in event of a fault.
6. Clocked serial command inputs.
7. Parity chink on command.
8. Internal 8 bit address decoding.
9. Power-cm reset option: ON or OFF.
10. Separate. command inputs:

Serial Command Port A	Serial Command Port B
Power-on Rc.set A	Power-on Reset B
SSPS Address A	SSPS Address B
Telemet try Enable A	Telemetry Enable B

11. Switch both sides of the. line.
12. Parallel operation supported.
13. Telemetry Outputs: Rc.side. in high impedance state unless enabled.

Digital:	ON/OFF A, 1 bit
	ON/OFF B, 1 bit
	OVERLOAD, 1 bit
Analog:	Load current
	Trip current

14. Design temperature range: - 30" C to + 85 "C.

PHYSICAL REQUIREMENTS

Max size:	2" x 2" x 3/8" or smaller when mounted, including leads.
Enclosure:	Low the.rmal impedance, metal case., flatpack style., with leads on two opposing sides of the. pac ka ge
Leads:	A minimum number of S4.
Mass:	30g typical or less. (NOTE: Final weight of a switch is about 31 to 32 gr)

IN HIT REQUIREMENTS

Bus Voltage:	30.0 ± 5.0 VDC
Logic Power A:	5.00 ± 0.2s VDC

BUS-SIDE PERFORMANCE REQUIREMENTS

PARAMETERS	TEST VALUES
On State Resistance (Ohms)	0.091 *to 0.192*
Turn On Time (ms)	200 ± 2s
Turn Off Time (ins)	400 ± 200
Trip Current (A)	4.0 ± 0.5
Trip Time (ms)	1.0 ± 0.2
Clamp Current (A)	6.0 ± 0.5
Leakage Current (mA)	0.1 max
Zene r Voltage (V)	43.0 ± 4.5
Timing Margin, Tch (ns)	300 max

RETURN . SIDEPERFORMANCE REQUIREMENTS

PARAMETERS			TEST VALUES
On State Resistance. (Ohms)			0.064 to 0.133
Turn On Tin, e (ins)			200 ± 25
Turn Off Time (Xs)			400 ± 200
Trip Current (A)			
SEL2	SEL1	SEL0	
0	0	0	0.600 ± 0.071
0	0	1	1,088 ±0.121
0	1	0	1 .s73 ±0.174
0	1	1	2.059 ±0.224
1	0	0	2.544 ±0.278
1	0	1	3.029 ±0.328
1	1	0	3.515 ±0.378
1	1	1	4.000 ±0.428

Trip Time (ins)	1.0 *0.2
Clamp Current (A)	6.0 ±0.5
Leakage. Current (mA)	0.1 rnax
Zener Voltage (V)	43.0 ±4.5
Load Current TLM (V)	2.40 ± 0.049
Trip Current TLM (V)	

SEL2	SEL1	SEL0	
o	0	()	0.194 ±0.043
o	0	1	0.390 ±0.055
0	1	()	0.s86 ±0.070
o	1	1	0.782 ±0.086
1	0	(1	0.978 ±0.104
1	0	1	1.174 ±0.121
1	1	0	1.37 ±0.139
1	1	1	1.567 ±0.157

Timing Margin, Tch (ns)	300 max

DIFFERENTIAL PERFORMANCE REQUIREMENTS

PARAMETERS	TEST VALUES
On State. Resistance (Ohms)	0.1s5 to 0.314
'rum On Time (ms)	87 to 225
Turn Off Time (Xs)	200 ±100
Trip Time. (ins)	1.0 ±0.2
Clamp Current (A)	6.0 ±0.5
Power Consumption (mW)	100 max
Load Voltage (V)	
V_{bus} = 25.0 ±0.025V	24.529 ± 0.496
V_{bus} = 30.0 ± 0.030V	29.529 ±0.501
v_{bus} = 35.0 ±0.035V	34.529 ±0.506
Digital Telemetry Output Levels (V)	
Logic O Level (I_{OI} - 50XA)	0.1 max
Logic 1 Level (I_{OH} = -50XA)	4.65 rnin

SS1'S HYBRIDIZATION

Following a long process of announcement of intent, RFP and a rigorous JPL Source Selection process a contract was placed in January of 1992 for the. hybridization of the JPL design. This was the. first known flight qualified hybrid to be fabricated in accordance and in compliance with MI L-11 -38 534A, K level requirements. All the components were procured to S level specification. Thus, element evaluation was performed to meet the. S level requirements. Four Hundred and Twenty-Four (424) flight qualified hybrids were dclivc.reel to JPL by 3/10/95.

Figure 2 shows both the JPL discrete implementation (9''X6.25° PCB) and the. hybrid (1 .99"X1 .6") side by side. To meet critical weight and volume requirements, the digital electronics (31 digital ICs) were. implemented by two redundant gate-arrays (the use of ASI C implementation was proposed by the selected hybridization contractor - CTSM of Indiana). The Gate-Array was designed and fabricated to specification by UTMC (Colorado). This was a semicustom chip CMOS Gate Array similar to the UTMC UT1 16 DR utilizing the supplier's 1.5 micron radiation-hardened CMOS process.Thestandard (library) flip-flop design was modified (by UTMC) to incorporate a triple modular design with a rnajority-vote scheme. This significantly increases the. single-event upset (SEU) immunity. It was determined that Boundary Scan was not needed as all the switch function were testable from the outside. This further reduced the probability of failure.. The. die was fabricated to S level requirements and certified to 100Krad total dose.. The Gate Array die. size is 0.236" ± 0.003" square.

Figure 2 depicts a view of the. assemble.d hybrid. The SSPS utilized a five. layered network on an Alumina (standard Al_2O_3) based substrate.. Dupont S704 was used as a dielectric. Conductor traces arc Gold. Resistors arc thick-film, Dupont Birox 1900. All the resistors were laser trimmed and twelve were dynamically trimmed to meet specified parameters. The SSPS FET dice were procured with a Gold backing to enhance attachment to the substrate. FET dice. were attache.d by Epoxy to a gold coated section of the. base Alumina substrate of the (5 layered) network. This further *improve.d* thermal performance for the FETs. Onc and 2 mil gold wire.s and 8 mil Al wires were used for bonding. Silver filled paste (Able Bond 84-l LMI-NB-I) was used to attache the components. The substrate was attached to the case with an Alumina filled Epoxy pre-form, Ablestick 570K- 1, 5mill thick. The SSPS is packed in a custom Kovar package (Made by Agis): (w) 1.680", (1) 1.995", (h) 0.170", with 72 glass scaled pins, and 0.40" thick walls. The hybrid is hermetically sealed.

SS1'S statistics:

1.	Number of active components (IC dice):	35
2.	Number of chip resistors and capacitors:	26
3.	Number of screened resistors: 12 rc.sisters arc actively trimmed	181
4.	number of wire bond: about 390 arc 1mil Gold	466

Six prototype units were. fabricate.cf for design verification. The sc units (two at a t ime) were tested both at CTSM and JPL. After some design modifications, twenty one units were fabricated by CTSM in a Mill-H-38534 K level line that was dedicated to the SSPS production. Eleven units were delivered to JPL for test ing and ten units were. placed on a 2000 Hour extended life test (at 125 °C). All together, twenty-three (23) units (the 10 from the first "batch" anrf the rest from subsequent flight-built units) were place.d on the 2000 Hours extended life-test. During this test the units were switched every half a second (On and Off alternately) under a 30mA load. All the units, with onc exception, passed the extended Ii fe-test. There were no catastrophic failures. The one. exception was a parameter anomaly i.e. a parameter that drifted out-of-spec after 1000 Hours of operation.

Extensive thermal analysis was performed on the hybrid design. Both two dimensional and 3D analysis indicated that the hybrid was well within the JPL derating criterion for worst case. Onc exception was the. worst case turn-on condition for the FETs. A pre dieted 133 "C peak junction temperature exceeded the JPL allowed 110 "C, for 700ms. After further analysis a waver was wr itten and approved. However, additional testing was also mandated. Six flight qualified units were tested by switching the m Off and ON at 300ms intervals under the maximum rated (sic.ady state) load of 3A. It was previously determined by analysis that this is a good representation of the worst case. This test was conducted for 8⅓ hours (100K state changes) while. maintaining the. case temperature at 75 "C. Additionally, two of the original six units were. selected for an additional onc million cycle test at room temperature under the maximum load of 3A. A 11 of the units passed the rc.fr.rc.need tests without an observable variation in electrical performance.. An IR view of the FETs was

also taken to identify "hot spots" (if any).. No anomalies were found and the detected temperatures were well below 100 "C.

The fabrication processes were governed by a detailed Traveler that was reviewed and approved by JPL. All the process documentation was reviewed and approved by JPL. In addition the. CTSM plant was surveyed for compliance with Ml L STD requi rements on three d i f fc.rent occasions. The late.st being an audit of the SS1'S MI L-11-38534A, K level dedicated line. This was conducted on June. 28,93 and was subsequently approved by July 14, 93.

A JPL Quality Assurance engine.er took up residency at CTSM for the entire. period of the production (of flight units). The QA engine.cr was responsible for ensuring that all of the quality and reliability provisions were met. He also had inspection, problem resolution, reporting, hardware. acceptance and other liaison responsibilities.

Following arc some of the. SSPS Traveler provisions:

Environmental conditions during the fabrication process

Operation	temperature(° C)		Time Exposure	
	M in	Max	Mirr	Max
Network Vat. Bake	130	170	12H	72H
Epoxy Cure (Device Attach)	9 S	105	60min	65min
	190	200	60min	65min
Epoxy Cure (Network attach)	95	105	60min	65min
	190	200	60min	65min
Preseal Burn-in	12s	135	8011	
Preseal Bake.-hybrids	150	160	2411	72H
Preseal Bake-lids	150	160	4H	72H
Vacuum Bake-hybrirk. & lids	185	195	6}1	12H
Part No. Stamping	150	160	50min	70min
Temperature cycling	125	130	10min (10 cycles)	
Burn-in	125	130	133H	
Burn in	125	130	133H (270H total)	

Through out the. fabrication process, with very few (three) exceptions, the SSPS was kept in a custom carrier (Azimuth 6151 B). This provided mechanical protection and kept the leads and structure out of harms way. All the. electrical testing, shipping and storage was done with the units in the.

Electrical Testing Provisions:

An extensive and comprehensive test plan and procedure was established for the SSPS. CTSM designed and built an automated test system that was equipped to test each unit over the entire operational envelope. The entire electrical test data package , for each unit, was provide.d in hard copy (paper) and on disk. JPL established a data base. for all the electrical test data.

The. SSPS was electrically tested at various stages of the fabrication process. The. first electrical test and verification was done. during the dynamic laser trimming of twelve (12) resistors. Trimming was performed at room temperature and at nominal voltage.s i.e. 30V bus and 5V logic. The load was varied as required try the trimming procedure.

Each SSPS was tested again after prc-seal burn-in. This was done at room temperature and nominal conditions. The test was repeated after scaling the unit,

A 100%, 270 hour burn-in followed. An electrical test, at nominal conditions, was performed at half point of the burn-in cycle. After completion of the. burn-in the units were tested over the entire voltage and temperature envelope. Voltages were: 2SV, 30V and 35V for the bus, 4.2SV, 5V and 5.25V for the logic supply. Tempera ture.s were: 2S "C, -20 "C and 75 "C.

THE NEXT GENERATION

The next generation of intelligent solid state spacecraft power switches will be driven by the requirements of faster, better, cheaper, and much smaller interplanetary spacecraft. While the Cassini spacecraft utilizes a 900 Watt power system with 192 SSPS's, the. next generation spacecraft, like Pluto Express or the Millennium missions, will utilize 50 to 100 Watt power systems and about 100 solid state. switches or less. The Cassini 3 1gr. SSPS must shrink while maintaining complex functionality that will support autonomous systems. Thus, ncw technologies and more innovative designs will be utilized. Mixed signal (analog and digital) ASIC technology will be used to obtain the highest possible level of integrat ion. New packaging techniques, utilizing High Density Interconnect processes that are applicable to power electronics must be utilize.d. The Pluto goal is to package four (4) independent power switches in a 15 cm^2 foot print (or smaller) package weighing less than 20gr. Additional design goals are: Flexible application, Zero OFF- state power consumption, output isolation and self contained logic power, all while maintaining the hard bus concept.

References

Da I ton, J, F., Clark, C, B., and Karmon, D., 1994, "Development of a Solid State Power Switch for the Cassini Spacecraft", 29th IECEC Conference. August 1994, AIAA-94-3961 -CP.

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JPL

SOLID STATE POWER SWITCH (SSPS) FOR CASSINI POWER SUBSYSTEM

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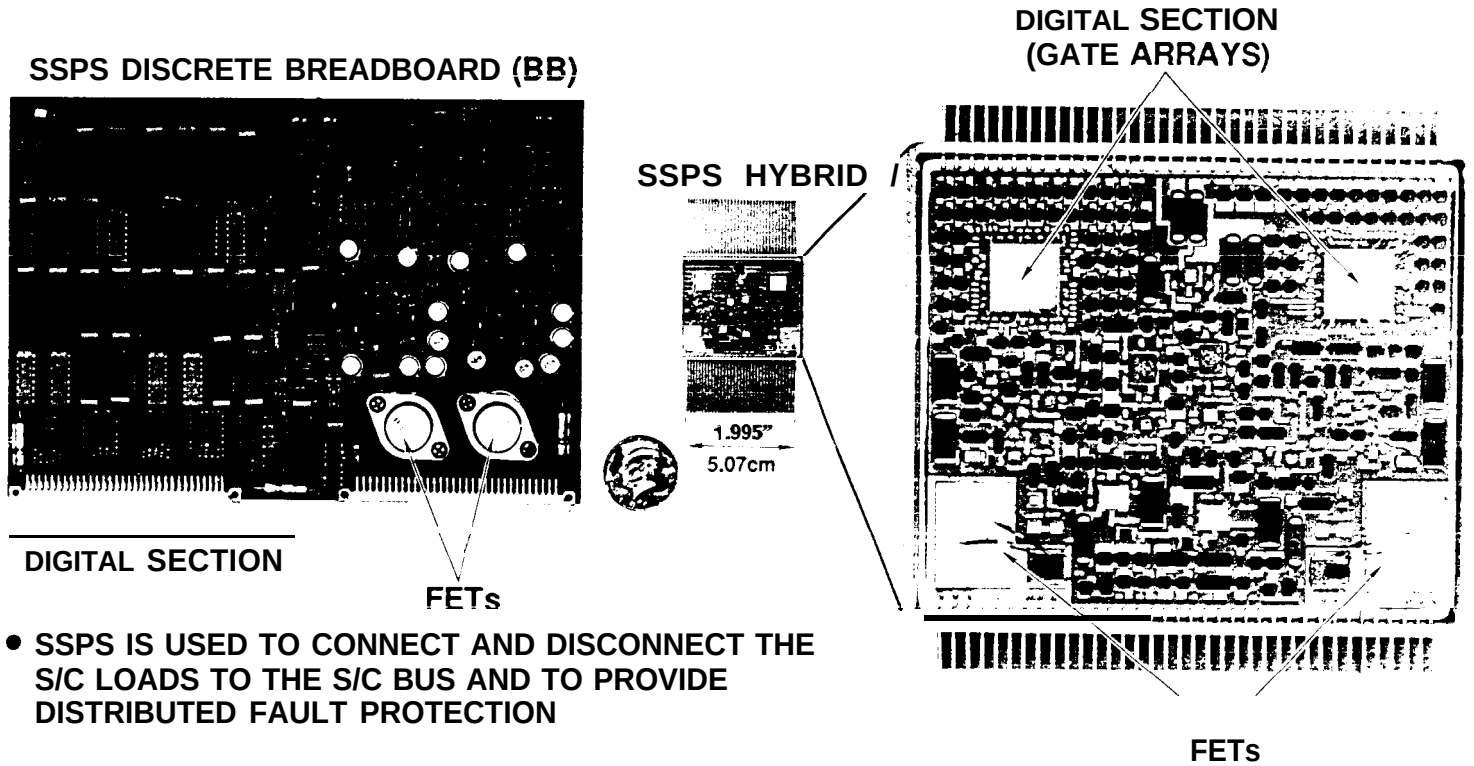

- SSPS IS USED TO CONNECT AND DISCONNECT THE S/C LOADS TO THE S/C BUS AND TO PROVIDE DISTRIBUTED FAULT PROTECTION
- FEATURES A REDUNDANT DESIGN FOR FAULT TOLERANCE
- RATED FOR THE 30V BUS AND 3A LOADS

Figure 2 SSPS Printed Circuit and Hybrid compared